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File   8:Ei Compendex(R) 1970-2003/Nov W4
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File  62:SPIN(R) 1975-2003/Oct W3
         (c) 2003 American Institute of Physics

Set      Items   Description
S1      195161   (ERROR? ? OR PARITY)(3N)(CHECK??? OR EXAM? OR TEST??? OR D-
              ETECT? OR ANALYZ? OR ANALYS?)
S2       51455   (SECOND? OR 2ND OR TWO OR DUAL? OR SEPARAT? OR DIFFERENT OR
               ANOTHER OR OTHER)(5W)(MEMORY OR MEMORIES OR RAM OR STORE OR -
              STORES OR STORAGE)
S3      169795   MULTIPLEX?
S4          11   S1 AND S2 AND S3
S5           9   RD (unique items)
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5/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06057656 E.I. No: EIP02216956418
Title: Design of a 3780-point IFFT processor for TDS-OFDM
Author: Yang, Zhi-Xing; Hu, Yu-Peng; Pan, Chang-Yong; Yang, Lin
Corporate Source: Department of Electronic Engineering Tsinghua University, Tsinghua, Beijing, China
Source: IEEE Transactions on Broadcasting v 48 n 1 March 2002. p 57-61
Publication Year: 2002
CODEN: IETBAC ISSN: 0018-9316
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0205W4
Abstract: This correspondence presents a design of 3780-point IFFT Processor for TDS-OFDM terrestrial DTV transmitter using FPGA. It demonstrates the algorithm design and **error analysis** of the processor, which can achieve a throughput of 7,56 M complex IFFT operations per second. This design meets the signal-to-quantization noise ratio requirement of the TDS-OFDM system. It consists of **two** FPGA and one **dual** -port **RAM** . The data stream pipeline algorithm is implemented. 13 Refs.
Descriptors: Digital signal processing; **Error analysis** ; Orthogonal frequency division **multiplexing** ; Digital television; Television transmitters; Random access storage; Pipeline processing systems; Field programmable gate arrays; Signal to noise ratio; Time domain analysis; Fast Fourier transforms; Algorithms; Optimization
Identifiers: Winograd Fourier transform algorithms (WFTA)
Classification Codes:
716.1 (Information & Communication Theory); 921.6 (Numerical Methods); 716.4 (Television Systems & Equipment); 722.1 (Data Storage, Equipment & Techniques); 722.4 (Digital Computers & Systems); 721.2 (Logic Elements); 921.3 (Mathematical Transformations); 921.5 (Optimization Techniques)
716 (Electronic Equipment, Radar, Radio & Television); 921 (Applied Mathematics); 722 (Computer Hardware); 721 (Computer Circuits & Logic Elements); 723 (Computer Software, Data Handling & Applications)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING)

5/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05050650 E.I. No: EIP98074264118
Title: 0.5 mu m CMOS circuits performing OFDM demodulation and channel estimation/correction for digital terrestrial TV applications
Author: Del Toso, C.; Combelles, P.; Penard, P.; Senn, P.; Sicre, J.-L.; Lauer, L.; Soyer, L.; Galbrun, J.; Scalise, F.
Corporate Source: France Telecom CNET, Grenoble, Fr
Conference Title: Proceedings of the 1998 IEEE 45th International Solid-State Circuits Conference, ISSCC
Conference Location: San Francisco, CA, USA Conference Date: 19980205-19980207
Sponsor: IEEE
E.I. Conference No.: 48558
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1998. IEEE, Piscataway, NJ, USA,98CH36156. p 38-39, 410 PAPER TP 2.5
Publication Year: 1998
CODEN: DTPCDE ISSN: 0193-6530
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 9808W4
Abstract: Two ICs resulted from DVBirds work. The first CMOS IC is dedicated to orthogonal FDM demodulation. The **second** , embedding 710 kb of

RAM , implements channel estimation and correction, a crucial issue in digital terrestrial TV applications. These two chips are intended for use in global chipset receiver specified for the DVBird European project, along with a channel decoder IC and a synchronization IC under development. 4 Refs.

Descriptors: CMOS integrated circuits; Frequency division **multiplexing** ; Demodulation; Communication channels (information theory); Digital communication systems; Television systems; Random access storage; **Error analysis** ; Synchronization; Decoding

Identifiers: Orthogonal frequency division **multiplexing** (OFDM)

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 716.1 (Information & Communication Theory); 716.4 (Television Systems & Equipment); 722.1 (Data Storage, Equipment & Techniques); 921.6 (Numerical Methods)

714 (Electronic Components); 716 (Radar, Radio & TV Electronic Equipment); 722 (Computer Hardware); 921 (Applied Mathematics)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

5/5/3 (Item 3 from file: 8)

01941019 E.I. Monthly No: EI8602012618 E.I. Yearly No: EI86060116

Title: DYNAMIC RAM CONTROLLER PUSHES SYSTEM SPEED TO 10 MHz - AND BEYOND.

Author: Meier, Webster; Garverick, Timothy

Corporate Source: Natl Semiconductor Corp, Santa Clara, CA, USA

Source: Electronic Design v 33 n 8 Apr 4 1985 p 205-208, 210, 212

Publication Year: 1985

CODEN: ELODAW ISSN: 0013-4872

Language: ENGLISH

Document Type: JA; (Journal Article) Treatment: A; (Applications)

Journal Announcement: 8602

Abstract: A description is given of a **second** -generator dynamic **RAM** controller, the DP8419, which can directly replace its predecessor, the DP8109, in most systems. Its higher speed is due to unusual delay line circuitry and to the bipolar oxide isolation process called advanced low-power Schottky. Moreover, its on-chip circuitry **multiplexes** addresses, generates control signal timing, and directly accesses up to 2 Mbytes of RAM. An extremely versatile chip, it interfaces with most popular microprocessors, and the addition of an **error detection** and correction chip (the DP8400-2) enhances the RAM system's data integrity. Like the earlier chip, the controller has all the dynamic RAM functions necessary to minimize skewing on its outputs. Built-in drivers are specified at 500 pF when driving 88 dynamic RAMs, and all ac and dc characteristics are guaranteed over the full range of operating temperature and supply voltage. The chip's nine address drivers enable it to directly drive 16-kbit, 64-kbit, and the newer 256-kbit dynamic RAMs.

Descriptors: *INTEGRATED CIRCUITS--*Applications; DATA STORAGE, DIGITAL--Random Access

Identifiers: INTEGRATED CONTROLLER; RAM ACCESS TIME; DATA INTEGRITY

Classification Codes:

714 (Electronic Components); 721 (Computer Circuits & Logic Elements)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

5/5/4 (Item 4 from file: 8)

01460126 E.I. Monthly No: EIM8312-087012

Title: SYSTEM-ORIENTED RAM CONTROLLER.

Author: Bazes, Mel; Nadir, James; May, Bradley A.

Corporate Source: Intel Corp, Santa Clara, Calif, USA

Conference Title: Northcon/82 Conference Record.

Conference Location: Seattle, Wash, USA Conference Date: 19820518

Sponsor: Electronic Conventions Inc, El Segundo, Calif, USA

E.I. Conference No.: 03047
Source: Publ by Electronic Conventions Inc, El Segundo, Calif, USA. Distributed by Western Periodicals Co, North Hollywood, Calif, USA Pap 14. 2, 11p
Publication Year: 1982
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8312
Descriptors: *DATA STORAGE, DIGITAL--*Random Access
Identifiers: DYNAMIC RAM CONTROL FUNCTIONS; ADDRESS **MULTIPLEXING** ; REFRESH CYCLES; ARBITRATION OF MEMORY REQUESTS; MICROPROCESSOR INTERFACE; MULTIBUS **DUAL** -PORT INTERFACE; **RAM** INTERFACE; **ERROR CHECKING** AND CORRECTION INTERFACE; RAM INITIALIZATION
Classification Codes:
722 (Computer Hardware); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING)

5/5/5 **(Item 1 from file: 35)**
DIALOG(R)File 35:Dissertation Abs Online

01867029 ORDER NO: AADAA-I3040466
Modeling, equalization and detection for two **-dimensional quadratic** storage **channels**
Author: Keskinoz, Mehmet
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: Carnegie Mellon University (0041)
Adviser: B. V. K. Vijaya Kumar
Source: VOLUME 63/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 425. 183 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544
ISBN: 0-493-53849-6

Volume Holographic Storage (VHS) is a promising digital storage technology because of its high data storage density, high data rate and short access times. The ability to **multiplex** several pages into a given volume of the material leads to potentially high densities. Also, VHS uses a highly parallel two-dimensional or page like format in recording and retrieval leading to high data rates. One way to increase the data density in a volume holographic storage channel (VHSC) is to use a frequency plane aperture and thus reduce the size of the effective recording area on the holographic medium. However, such frequency plane aperturing causes severe inter-symbol interference (ISI) leading to poor bit-error rate (BER) performance. In addition to ISI, optical and electronic noise affect the BER adversely and thus limit the capacity of the VHSC. Equalization and detection methods should be employed to mitigate the effects of ISI and noise and to increase the storage capacity. However, the VHS output detector array detects the <italic>intensity</italic> of the incident light wavefront and this results in sign information loss due to the quadratic nonlinearity. This sign loss prevents the applicability of conventional equalization/detection schemes used in 1-D magnetic and optical storage channels. The goal of this thesis is to develop and evaluate equalization and detection methods for such quadratic storage channels.

In this thesis, we first address channel modeling under quadratic nonlinearity. We then design and analyze various equalization/detection methods using this quadratic channel model. We first derive a simple linear equalization technique, namely linear minimum mean square (LMMSE) equalization and then consider the applicability of more advanced methods based on decision feedback and partial response maximum likelihood. The performance of equalization/detection methods is quantified in terms of equivalent density gain offered for optical noise dominated channel as well as electronic noise dominated channel. We show that iterative magnitude square decision feed back equalization (IMSDFE) is the most promising method for high-density and high-ISI VHSC. We also evaluate the effect of modulation coding, particularly balanced codes and low pass coding, and

magnification **error** on the equalization/ **detection** performance. These results indicate that (LMMSE + 6:8 balanced code) and (IMSDFE + low pass coding) are good candidates for high-density, high-ISI VHSC with magnification errors.

5/5/6 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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1399713 NTIS Accession Number: PB89-103725
Personal Computer Field Site Data Acquisition System Operating Manual. Topical Report January 1986-December 1987
Malcosky, N. D. ; Clay, P. A. ; Herchline, L. E. ; Kerr, G. H.
Columbia Gas System Service Corp., Columbus, OH. Research Dept.
Corp. Source Codes: 006700001
Sponsor: Gas Research Inst., Chicago, IL.
Report No.: GRI-88/0254
Jul 88 186p
Languages: English
Journal Announcement: GRAI8901
Sponsored by Gas Research Inst., Chicago, IL.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A09/MF A01
Country of Publication: United States
Contract No.: GRI-5086-242-1210
The Research Department of the Columbia Gas System Service Corporation has developed a personal computer based site data acquisition system (DAS), and a modular data acquisition software package, including specific modules for acquisition of data from gas engine heat pumps, and real time calculation of COP. The DAS hardware and software have been implemented at 12 field test sites nationwide, acquiring data from 1.8RT - 4RT gas engine heat pumps. The DAS consists of an IBM personal computer (or 100% compatible clone); MetraByte data acquisition, counter/time and analog **multiplexer** /amplifier boards, EDA constant current power supply and pulse train 'Debounce' boards; and a Hayes 1200 baud modem. The software consists of the Columbia-designed, modular data acquisition, engineering unit conversion, data analysis, data display and data storage routines, and KTALK file dispatcher with bi-directional communication and **error checking** routines. The system stores operating system, data acquisition/analysis and communications software on one floppy disk drive, and stores data in 60 kb data blocks on a second floppy disk drive. The system scans up to 138 sensors every 15 **seconds** , and **stores** averaged data to disk every 15 minutes, or on every change in heat pump operating mode.
Descriptors: *Gas heat pumps; Gas industry; Tables(Data); Graphs(Charts); Field tests; Monitoring; Telephone lines; Data transmission; Personal computers; Random access memory
Identifiers: Disk recording systems; IBM PC/XT computers; DAS computer program; BASICA programming language; NTISGRI
Section Headings: 97J* (Energy--Heating and Cooling Systems); 94GE (Industrial and Mechanical Engineering--General)

5/5/7 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS
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0676872 NTIS Accession Number: UCRL-80053/XAB
Multi-Access Storage Subnetwork
Wentz, D. L.
California Univ., Livermore. Lawrence Livermore Lab.
Corp. Source Codes: 9500007
Sponsor: Energy Research and Development Administration.
Report No.: CONF-770937-1

7 Sep 77 20p
Document Type: Conference proceeding
Journal Announcement: GRAI7807; NSA0300
ERDA/AESOP 17, Boston, Massachusetts, USA, 13 Sep 1977.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Contract No.: W-7405-ENG-48
The Multi-Access Storage Subnetwork is the latest addition to the Octopus Computer Network at Lawrence Livermore Laboratory. When in production in early 1978, the Subnetwork will interface a Control Data Corporation 38500 Mass Storage Facility System to the host worker computers. This will provide an on-line capacity of 1 x 10 exp 12 bits of user storage. The MASS architecture provides a very high performance approach to the management of MASS Storage, as well as a high degree of reliability needed for operation in the Laboratory's time-sharing environment. The LLL-designe subsystem combines state-of-the-art digital hardware with an innovative system philosophy. The key design features of the subnetwork which contribute to high performance include a data transmission scheme which provides a 40-megabit-per-second channel over distances of up to 1,000 feet to link MASS with the worker computer disk systems; a 280-megabit-per- **second** , 24-port **memory multiplexor** controlling a large MOS memory used for intermediate buffer between the computers and the Mass Storage; and a set of high-speed microprocessor-based controllers driving the commercial Mass Storage units. Reliability of the system is provided by a completely redundant network including two control minicomputer systems. Also enhancing reliability is **error detection** and correction in the MOS buffer. A 64-bit hardware-generated checksum is carried with each file throughout the entire network, insuring integrity of user files being transferred via MASS. 10 figures. (ERA citation 03:007795)
Descriptors: *Magnetic storage devices; Design; Joining; Lawrence livermore laboratory
Identifiers: *OCTOPUS computer network; *Computer architecture; ERDA/990200; Microprocessors; NTISDE
Section Headings: 62A (Computers, Control, and Information Theory--Computer Hardware)

5/5/8 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

0279491 NTIS Accession Number: AD-726 534/XAB
Graphics
(Semiannual technical summary rept. 1 Dec 70-31 May 71)
Forgie, J. W.
Massachusetts Inst of Tech Lexington Lincoln Lab
Corp. Source Codes: 207650
Report No.: ESD-TR-71-151
31 May 71 25p
Journal Announcement: GRAI7117
See also AD-689 782.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Contract No.: F19628-70-C-0230; ARPA ORDER-691
The hardware for the Terminal Support Processor (TSP) system is in various stages of design, construction, and checkout. The two Digital Scientific Corporation Meta 4 microprocessors and main memory system have been delivered, but acceptance awaits the installation of revised memory controller and central processor boards. The **secondary memory** has been delivered to the interface vendor, and the interface has been checked out on a single processor system. A multichannel controller which will simplify the interfacing of the other peripheral equipment has been constructed and

tested. A serial transmission and time **multiplexing** scheme for handling keyboards and console indicators has been designed. The design uses a standard TV composite video signal. Two minimal console stations have been built and **tested** . **Error** rates appear to be satisfactory for this application. TSP software effort has concentrated on developing the support facilities which run on TX-2 and handle assembly and compilation for the TSP. Code generators for a BCPL compiler for the BCOM machine, the processor for system software in the TSP, are being debugged and indicate good efficiency of compiled code. Diagnostics for the BCOM machine have been written and debugged on the Meta 4 simulator on TX-2 and have been tested satisfactorily in the Meta 4 system. (Author)

Descriptors: Data processing systems; *Graphics; *Programming(Computers); Display systems; Compilers; Computer storage devices; Digital computers; Interfaces; Time sharing; Coding; **Multiplex**

Identifiers: *Computer graphics; TX2 computer; Microprogramming; Central processing units; LX1 microprocessor; NTISAF

Section Headings: 62A (Computers, Control, and Information Theory--Computer Hardware); 62B (Computers, Control, and Information Theory--Computer Software)

5/5/9 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

07144089 Genuine Article#: 128PN Number of References: 55

Title: Interleaving and error correction in volume holographic memory systems

Author(s): Chou WC (REPRINT) ; Neifeld MA
Corporate Source: UNIV ARIZONA,DEPT ELECT & COMP ENGN/TUCSON//AZ/85721 (REPRINT)

Journal: APPLIED OPTICS, 1998, V37, N29 (OCT 10), P6951-6968
ISSN: 0003-6935 Publication date: 19981010
Publisher: OPTICAL SOC AMER, 2010 MASSACHUSETTS AVE NW, WASHINGTON, DC 20036
Language: English Document Type: ARTICLE
Geographic Location: USA
Subfile: CC PHYS--Current Contents, Physical, Chemical & Earth Sciences; CC ENGI--Current Contents, Engineering, Computing & Technology
Journal Subject Category: OPTICS

Abstract: We study the use of error-correction coding (ECC) and **two** -dimensional interleaving for volume holographic **memory** (VHM) systems suffering from both random and systematic errors. The bit-error rate (BER) is used as the data-fidelity measure and as a design metric for optical 4f systems. The correlated error patterns arising from both lens aberrations and misalignment **errors** are **analyzed** , and we discuss the information theoretic storage capacity of VHM in the presence of such correlated error patterns. The performance of interleaving and ECC is analyzed from both BER and storage-capacity perspectives. Magnification, rotation, tilt, and defocus errors are also studied, and an experimental demonstration that combines ECC with two-dimensional interleaving is included. (C) 1998 Optical Society of America.

Identifiers--KeyWord Plus(R): CROSS-TALK NOISE; DATA-STORAGE; OPTICAL MEMORIES; PHOTOREFRACTIVE MEMORIES; **MULTIPLEXED** HOLOGRAMS; PAGE-ACCESS; CAPACITY; ERASURE; CODES; REDUCTION